IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
David J. Cocca	Group Art Unit: 2124
Application No.: 09/896,780	Examiner: TRENTON J ROCHE
Filed: June 29, 2001	Confirmation No.: 8893
For: METHOD AND APPARATUS FOR DYNAMICALLY MODIFYING A STORED PROGRAM	

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated October 7, 2004, Applicant respectfully requests reconsideration and withdrawal of the rejection of the claims. The Examiner is thanked for his courteous discussion with Applicant's undersigned representative, during which he further explained his interpretation of the claim language relative to the disclosure of the *Koskal et al.* patent.

In the most recent Office Action, the rejection of all pending claims as being anticipated by the *Koskal et al.* patent was repeated. As pointed out in Applicant's previous response, the *Koskal et al.* patent does not anticipate the claim subject matter since it does not disclose, among other features, that the program to be corrected and the correction code are stored in the same memory, specifically the same electrically erasable programmable memory.

In response to this argument, the most recent Office Action asserts that there is no language in claim 1 that states that the program to be corrected and the patch code reside in

the same memory. The Office Action states that the claim only requires that the correction code be stored in the electrically erasable programmable memory, and further that a program having instructions be stored in the same electrically erasable programmable memory. As explained by the Examiner in the above-referenced discussion, this claim language does not require that the program stored in the memory be the same as the program to be corrected by the correction code.

It is respectfully submitted, however, that the nexus between the correction code and the program stored in the memory is set forth in the third step of claim 1, which recites "invoking an address match routine to execute at least a portion of the correction code *in place of* at least one of the instructions during the executing of *the program.*" (emphasis added). Since the claim only identifies one program, the recitation of "the program" in this clause must necessarily refer to the claimed "program having instructions stored in the memory" recited in the preceding step. Furthermore, since the third step recites that a portion of the correction code is executed "in place of" instructions during the executing of that program, it is respectfully submitted that the claim explicitly defines that the program being corrected is the one that is stored in "the memory". The claim also recites that the correction code is stored in the same memory.

Accordingly, it is respectfully submitted that, when the claim is read as a whole, it clearly defines that the correction code and the program that is corrected by this code are stored in the same electrically erasable programmable memory. In contrast, the *Koskal et al.* patent discloses that the patch code and the program code corrected by the patch code are stored in two different memories. Specifically, the program code is stored in the internal ROM 108 (column 6, lines 22-23), i.e., non-writable memory, whereas the patch

code is stored in a "second" memory such as the external ROM 114 or the NVRAM 112 (col. 7, lines 1-3). Since the *Koskal et al.* patent discloses that the program code is stored in a non-writable ROM, it is more analogous to the *Yamaguchi et al.* patent discussed on pages 1 and 2 of the present application. It does not disclose that both the program to be corrected and the correction code are stored in the same electrically erasable programmable memory.

For at least this reason, therefore, it is respectfully submitted that the subject matter of claim 1 is not anticipated by the *Koskal et al.* patent. For the same reasons, claim 17 is not anticipated.

Another distinguishing feature of the invention, discussed in Applicant's previous response, is recited in claims 6-10. Claim 6 depends from claim 2 and recites further steps including, among others, "retrieving a second data value from each of the correction blocks... [and] comparing the retrieved second data value...to a post address match value of the program counter." In responding to Applicant's arguments regarding these features, the most recent Office Action states that the claim language is interpreted to be a first comparison of data values, and refers to the *Koskal et al.* patent at column 13, lines 3-6. This portion of the patent states that the contents of the program counter stored on the stack is compared with the patch address to determine if the address stored on the stack is the next sequential location following the patch address.

It is noted that this same subject matter was identified in connection with the rejection of claim 2, which recites that an address match routine is invoked when a program counter associated with the executing of the program matches at least one of the plurality of address match registers. In other words, the Office Action is referring to the same subject

matter in the *Koskal et al.* patent as disclosing the matching recited in claim 2 and the comparing step recited in claim 6. However, it is to be noted that claim 6 depends from claim 2 and recites the "further" steps of "retrieving..." and "comparing..." In other words, the comparing step of claim 6 is *in addition to* the matching recited in claim 2, i.e. it is a separate operation. For example, with reference to the disclosed embodiment, the matching recited in claim 2 occurs at step 503 in Figure 5. If a match is detected, the process moves to the subroutine of step 505, which is depicted in Figure 6. Within this subroutine, the comparing step of claim 6 is carried out at step 607.

As such, the *same* procedure disclosed in the *Koskal et al.* patent cannot be interpreted to anticipate *both* of the two separate operations recited in claims 2 and 6. At best, it can only be interpreted to relate to the subject matter of claim 2, in which case it does not anticipate the subject matter of claim 6.

Claim 34 recites a memory map structure that is electrically erasable programmable memory based. One of the claimed elements of the memory is a main program area for storing at least one executable program. In connection with this subject matter, the Office Action refers to internal ROM 108 of the Koscal patent. However, this ROM is not an electrically erasable programmable memory, and therefore cannot be a component of a memory map structure that is based on electrically erasable programmable memory.

Another elment of the memory recited in claim 34 is an initialization area for storing code to enable an address match interrupt. With reference to this subject matter, the Office Action refers to element 142 of the Koscal patent. However, this element is not a component of the *memory*. Rather, it is disclosed as a compare *circuit* having three inputs

and one output, i.e. it is a separate hardware structure. There is no disclosure that this circuit stores code, as recited in the claim.

Claim 34 also recites a vector table for triggering the address match interrupt. The Office Action refers to element 302 of the Koscal patent in connection with this claimed feature. Element 302 is disclosed as the area where the patch address is stored (column 11, lines 3-4). This patch address is the starting address where the patch code resides. This is the address to which the processor jumps when a software trap occurs. There is no disclosure that this patch address functions to "trigger" an address match interrupt, as recited in the claim. Rather, this address is not accessed until *after* the interrupt occurs.

In view of theses differences, it is respectfully submitted that the Office Action has not established that the Koscal patent anticipates claim 34.

For at least the foregoing reasons, therefore, it is respectfully submitted that the presently pending subject matter is not anticipated by the *Koskal et al.* patent. Reconsideration and withdrawal of the rejection is therefore respectfully requested.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

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By: 

James A. LaBarre
Registration No. 28,632

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620